

ABSTRACT OF THE DISCLOSURE

An improved method, structure and process flow for reducing line-line capacitance using low dielectric constant (K) materials is provided. Embodiments in accordance with the present invention form structures for semiconductor devices having a single level of
5 interconnection as well as semiconductor devices having multiple levels of interconnection.

In embodiments of the present invention, an initial dielectric structure is formed having a first low K material overlaid with a standard K material. In subsequent processing, conductive interconnects are formed and the standard K material replaced with a second low K material. In some embodiments of the present invention, the first and second low K
10 materials are the same material, in some embodiments the first and second low-K materials are different materials. Embodiments of the present invention having multiple levels of conductive interconnects are formed by employing methods and materials analogous to those used to form the first level of conductive interconnect and dielectric material disposed therebetween. Embodiments of the present invention employ low K materials formed by
15 spin-on processes as well as low K materials formed by CVD processes.